DESIGN OF A QPSK MODULATOR FOR ISM BAND MODEMS

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Abstract

In this article, the design approach and performance characteristics of a 200 Mbps QPSK modulator operating at 5.8 GHz are presented. The modulator, aiming to be used primarily in wireless modems operating at microwave frequencies, is implemented as a low cost hybrid microwave integrated circuit (MIC) sized 37.5 mm by 33.5 mm.

1. INTRODUCTION

In system level, a typical QPSK modulator shown in Figure 1, can be configured by use of a 90° coupler, two balanced (BPSK) modulators, and a power combiner [1]. The quadrature coupler, operating both as a power splitter and as a phase shifter, provides two mutually orthogonal carriers from a single oscillator. The quadrature carriers are applied then to a pair of balanced modulators along with the I and Q bit streams of data. The QPSK waveform is finally obtained as a Quadrature Multiplexed signal, by combining the quadrature BPSK signals from balanced modulators, in a power combiner.

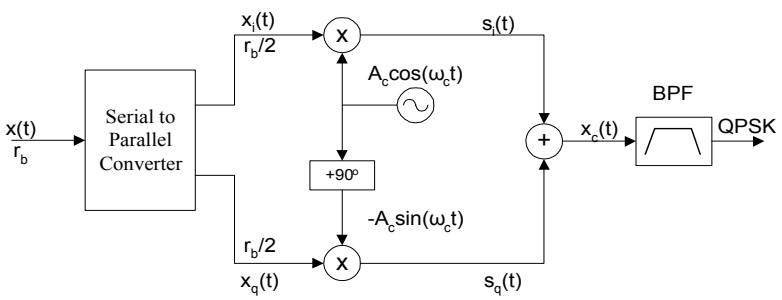


Figure 1. Block diagram of QPSK modulator.

Due to the market strong interest on high rate wireless modems, the main effort in this task aimed at the development of a low cost MIC with moderate size and performing as a high data rate QPSK modulator at ISM band frequencies. The modulator of present design operating at 5.8 GHz with 200Mbps data rate is shown in

Figure 2. It has been implemented by a 37.48 mm × 33.5 mm hybrid microstrip circuit and the occupied area is 1257.6 mm^2.

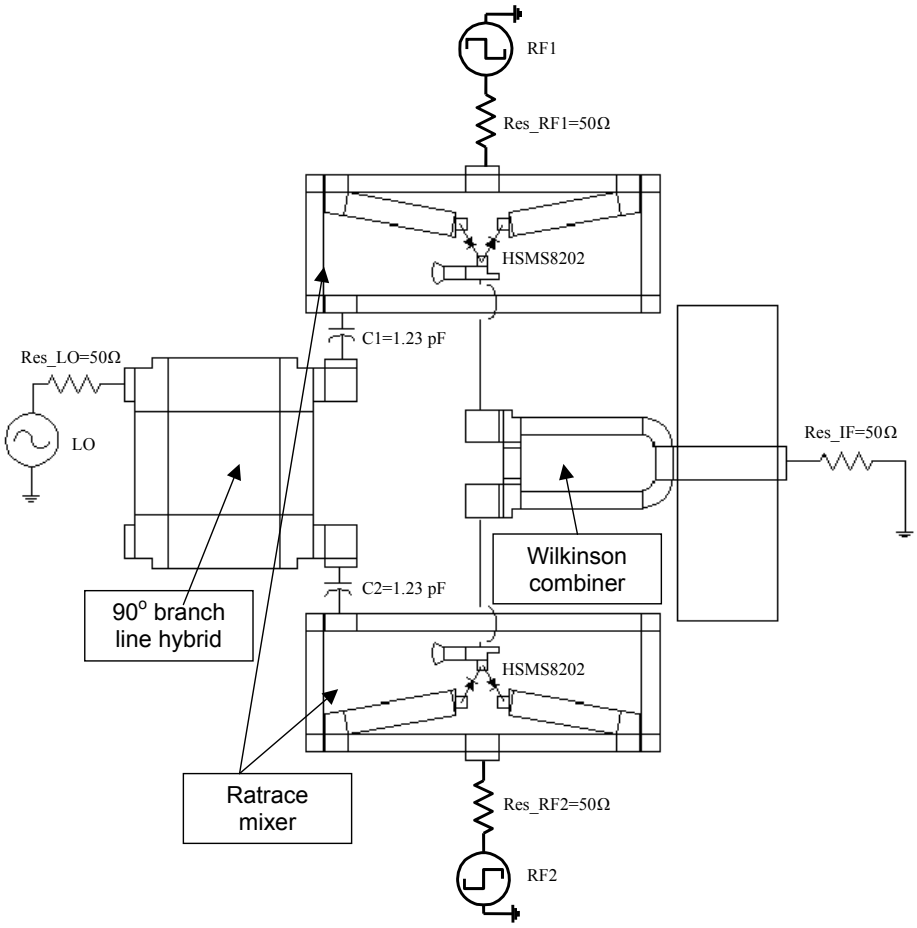


Figure 2. Circuit of QPSK modulator.

In this article, the basic steps in the design of the QPSK modulator are summarized. In the next sections, a description of the circuit is given and issues concerning the implementation of modulator in circuit form are illustrated. Furthermore, test procedures applied to the assembled QPSK modulator are discussed and results concerning performance of the module are presented.

2. DESCRIPTION OF THE CIRCUIT

As it was previously indicated, the main blocks of the QPSK modulator are the 90° directional coupler, the Wilkinson divider/combiner and the passive balanced mixer (or

modulator). In the modulator of Figure 2, the carrier generated by an oscillator operating at f_c=5.8 GHz is applied to the input of a Quadrature (90 degrees) Directional Coupler. The coupler has been implemented as a typical microstrip branch line coupler with quarter wavelength lines [2]. The quadrature carriers from coupler are applied then to a pair of balanced modulators along with the bit streams of data. The data rate of input polar pulses in both upper and lower balanced modulator is 100 Mbps, resulting in a bit rate of 200 Mbps for QPSK modulator. The balanced modulators have been implemented [3, 7] as passive singly balanced mixers by use of rat-race hybrids and Schottky diodes. Conversion loss had to be tolerated during circuit optimization in order to reach an acceptable level. Rat-race hybrid permits placement of diodes and associated matching circuit inside its loop. With respect circuit miniaturization, this property of rat-race hybrid was ranked high in selecting the specific type of mixer. As diodes, the HP device [5] HSMS–8202 has been selected. The chip contains a pair of series connected Schottky diodes, which are appropriate for mixer applications, and it is offered in a surface mount package that is suitable for a MIC implementation. The desired QPSK output is obtained by combining the orthogonal BPSK signals from mixers in a Wilkinson power divider/combiner with $\lambda/4$ lines [2]. It should be noted that the addition of $\lambda/4$ short-circuited stubs at the output of the combiner improved significantly the performance of the system. That was realized during optimization and trimming of the finally assembled modulator circuit, when the presence of stubs at output port improved efficiency by minimizing the conversion loss and increasing the power level of desired spectral components in the QPSK output. In addition, the presence of stubs at the output of power combiner also served the necessary filtering of undesired products contained in the output of mixers. Thus it was concluded that additional filter at the output of the modulator was not needed. Viewing this fact from the miniaturization point of view it was considered as a benefit. The size of the final assembled circuit, on a Rogers RO4003 substrate [6] with 0.81 mm thickness and 17μm copper foil cladding, is 37.48 mm by 33.5 mm ≈ 1257.6 mm^2.

3. DESIGN NOTES ON MODULATOR DEVELOPMENT

The development of QPSK modulator followed a stepped (one at a time), top to bottom (from system level to circuit level), design strategy. For each building block and sub-circuit of the modulator, several alternative implementations were investigated, examined and tested independently. As a rule, the final selection was based on

requirements concerning simplicity, implementation cost and required vs. available space. It should be pointed out that, no significant gain has been obtained in present microstrip implementation, when several well-established miniaturisation techniques (e.g. shortening of λ/4 lines by use of capacitors or by bending lines) was tried to be adopted. By the way, such techniques have been widely used and are very effective in the design of MMICs. For similar reasons, it was not preferred the selection of an active mixer in the design of BPSK modulators.

The design of QPSK modulator performed, checked and optimized in PCs, using the HP-Eesof Libra version 2.20. For layouts, the TS2ACAD of Artwork Conversion Software, Inc was used. Since Libra version 2.20 does not support schematic editing we also used in some cases the Protel Advanced Shematic 2.0.4 program.

Next, the design of the basic building blocks of the modulator is presented. That is the 90 degrees directional coupler, the Wilkinson divider/combiner and the passive balanced mixer.

3.1 BRANCH LINE HYBRID

Quadrature Directional Coupler had to meet basic specs concerning design frequency (5.8 GHz), return loss (>20 dB), isolation between output ports (>30 dB) and tolerances in equal power division between outputs (±0.3dB). In addition, a $90^o \pm 5^o$ phase difference between output ports was also specified, as acceptable. A microstrip branch line hybrid was selected and the circuit schematic (Figure 3a), introduced in Libra for simulation and optimization. The optimization goals obtained from specs were 30dB minimum for both return loss and isolation in the frequency region 5.78 – 5.82 GHz, an equal power splitting with less than ±0.3dB tolerance and a 90° phase difference between outputs at 5.8 GHz. As optimization variables were selected the lengths (LA, LB) and widths (WA, WB) of quarter wavelength lines, resulted in LA=6.051 mm, WA=3.022 mm for the series arm λ/4 lines (Z_r=35.36Ω) and LB=7.197 mm, WB=1.85 mm for the shunt arm λ/4 lines (Z_p=50Ω). The s-parameters of the circuit are shown in Figures 3b and 3c.

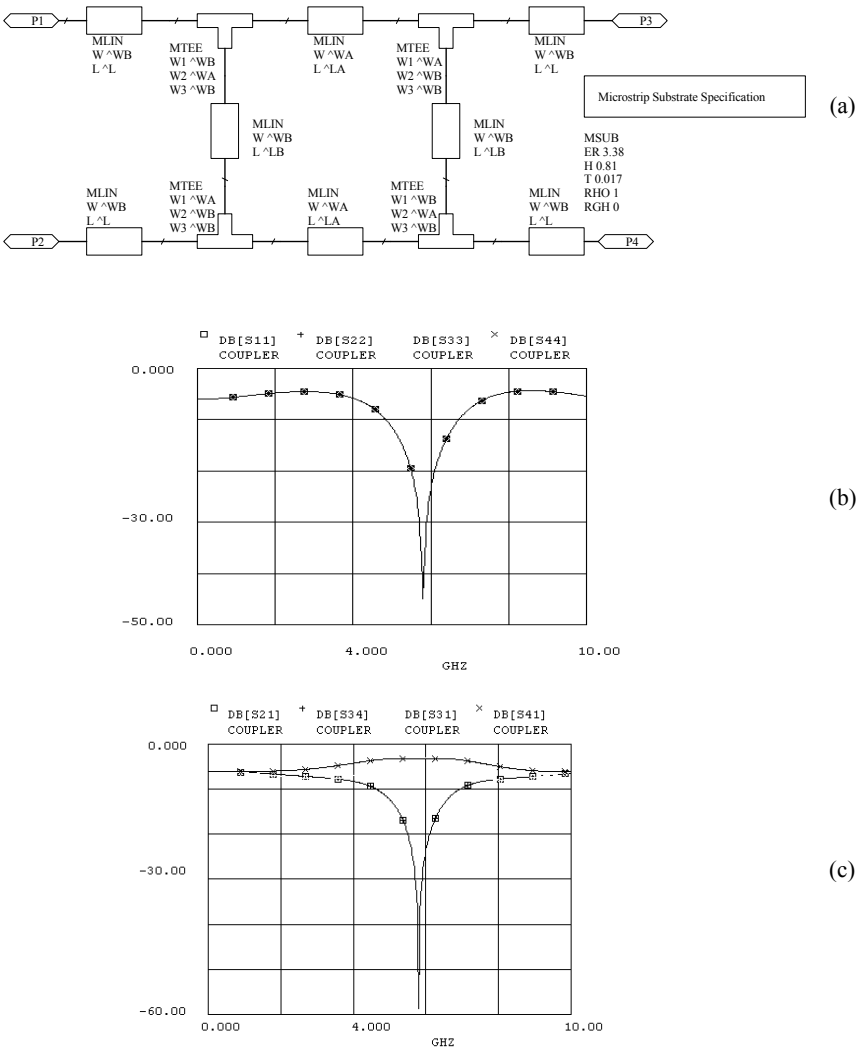


Figure 3. Branch Line Coupler (a) Schematic (b) Return Loss (c) Insertion Loss vs. frequency

3.2 WILKINSON COMBINER/DIVIDER

Power combiner also had to meet basic specs concerning design frequency (5.8GHz), required bandwidth (200MHz), return loss (>20 dB) and isolation between output ports (>30dB). In addition, no tolerances were permitted in power division and phase difference between output ports. After some trials, it was selected a Wilkinson combiner/divider with quarter wavelength lines, and the circuit schematic (Figure 4a), introduced in Libra for simulation and optimization. The optimization goals obtained from specs were 40dB minimum for both return loss and isolation, an equal power splitting and 0° phase difference between outputs, in the frequency region 5.78 – 5.82 GHz. As variables were selected the lengths LA and LT of quarter wavelength microstip

lines and thin-film resistor, respectively. The optimization resulted in LA=7.447 mm, LT=0.884 mm and the width of thin film resistor is WB=0.5mm. The s-parameters of the combiner are shown in Figures 4b and 4c.

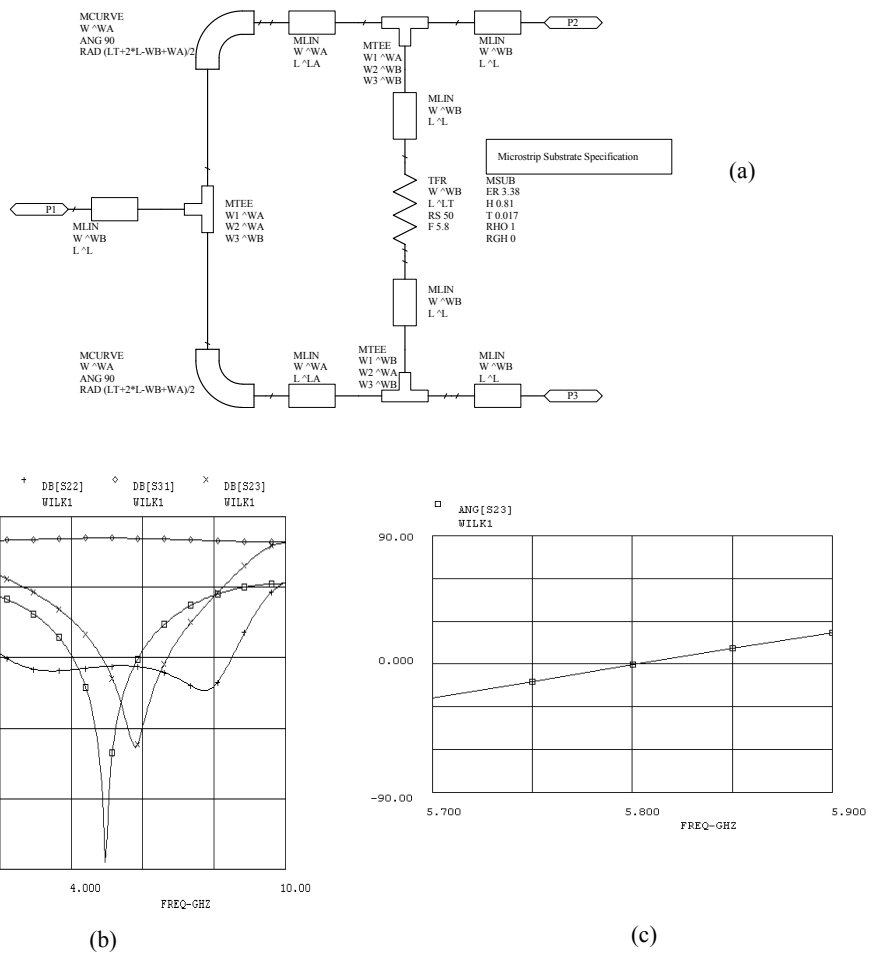
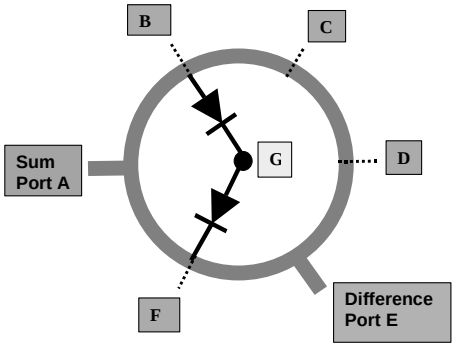


Figure 4. Wilkinson Power Combiner with λ/4 lines (a) Schematic (b) S-parameters and (c) Phase difference between output ports vs. frequency.

3.3 BPSK MODULATOR (SINGLY BALANCED RAT-RACE MIXER)

BPSK modulation is obtained as a mixing process. For this purpose, a passive singly balanced rat-race mixer has been designed. It is a low cost mixer with low power demands from LO source. Mixer operates as an up-converter [4] producing a BPSK signal. In Figure 5a, is shown a model of mixer. The necessary mixer components are a rat-race hybrid, and a pair of Schottky diodes with the associated matching circuits. In Figures 5b and 5c, are shown the model and the layout of rat-race hybrid, while design

steps are summarized in Table 1 and s-parameters variations vs. frequency, are plotted in Figure 6.



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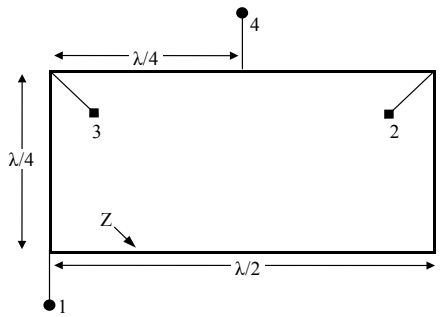

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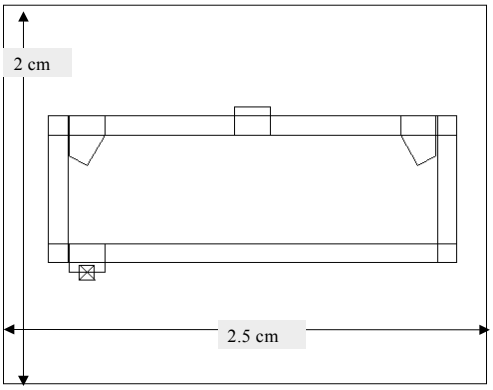


(c)

Figure 5. (a) Model of mixer (b) Model and (c) Layout of rat-race hybrid.

Table 1. Design of rat-race hybrid

Specifications
Design frequency f_c=5.8 GHz.
Bandwidth: 200 MHz
Return loss of ports : >20 dB
Tolerance of input power separation between outputs : ±0.5 dB
Phase difference between output ports : $0^o \pm 10^o$ for sum port input and $180^o \pm 10^o$ for difference port input
Isolation between I/O ports : >30 dB
Characteristic Impedance of ports Z_o=50 Ω
Simulation and Optimization
Optimization Goals
Return loss : >20dB in the 5.7 – 5.9 GHz band
Isolation : >20dB from port 1 to 4 and 3 to 2 in the band 5.7 – 5.9 GHz
Phase difference between ports : 90° between 2-3, -90° between 1-4
Insertion loss : 3dB from port 1 to 3 and 4 to 2
Optimization Variables
Lengths LA and LC of quarter wavelength microstip lines
Results
Length of quarter wavelength microstip lines LA=6.72988 mm and LC= 5.74276 mm
Width of quarter wavelength microstip lines WA=1 mm

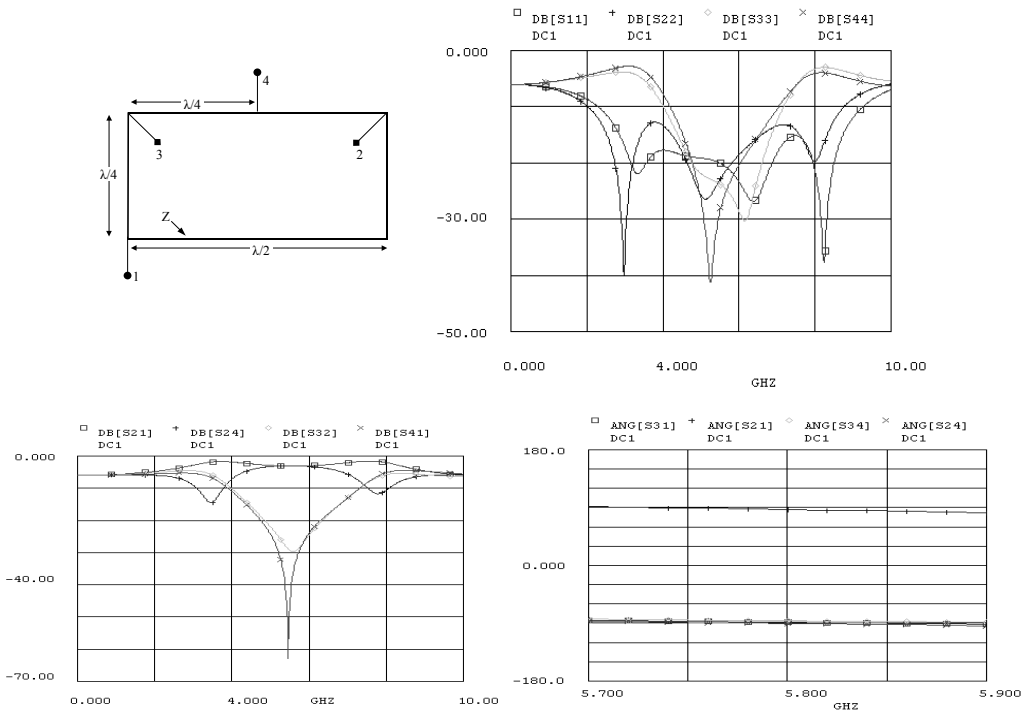
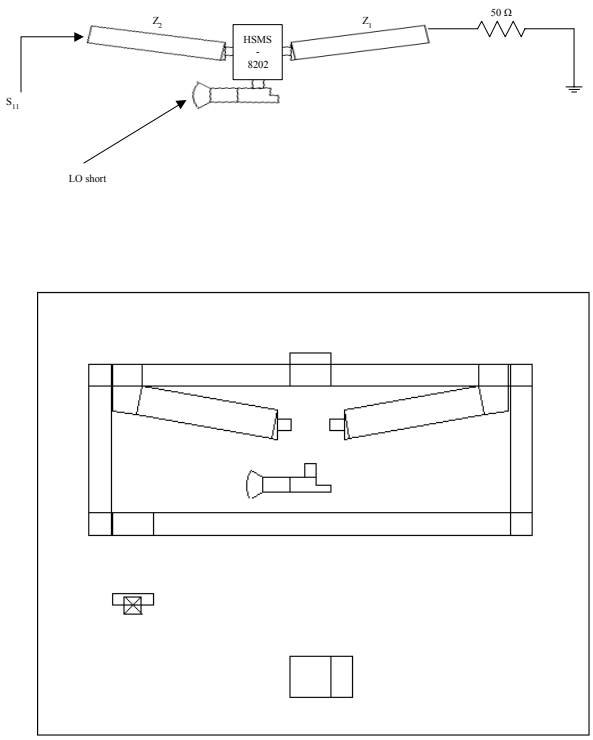


Figure 6. S-parameters of the rat-race hybrid

3.3.1 MATCHING CIRCUIT FOR DIODES

In the mixer model of Figure 5a, diodes are connected directly to points B and F of the hybrid. In practice, a matching circuit for diodes is needed, since the common point G must present low impedance at LO frequency, and in addition, the diodes have to be properly matched with rat-race hybrid, in the frequency range of interest. The matching circuit of Figure 7a, consists of a radial open circuited stub along with sections of microstrip lines. It contains two line sections with L=6.23 mm and W=1.33 mm connecting each diode to hybrid, and at the common output point, a section with L=1.26 mm and W= 0.69 mm along with a radial stub with 0.6 mm radius and 60.98^{o} angle. Device modeling including package parasitics introduced in Libra both for linear and non-linear operation of HSMS–8202 diodes [8]. It is noticed that information about device modeling is critical and in our case it was obtained from vendor sites through Internet.



(a)

(b)

Figure 7. (a) HSMS–8202 with associated matching circuits (b) Layout of rat-race mixer.

In the finally assembled mixer (Figure 7b), the diodes are connected to rat-race hybrid through the matching network. For sum port input (RF port) a direct connection

is used while the difference port (LO port) is ac coupled by use of a 1.23pF chip capacitor, which improved isolation between RF and LO ports. The common node of diodes (IF port) is connected to the Wilkinson combiner by use of a small piece of a wire over substrate.

4. TESTING AND IMPROVING MIXER PERFORMANCE

For mixer optimization, the harmonic balance capability of Libra was used. By applying a LO power sweep the mixer conversion loss was checked. Thus an optimum +4 dBm LO power level was selected. Next, return loss and isolation were examined and IF output power spectrum was also observed for levels of desired and undesired harmonics and resultant carrier compression. Optimization goals introduced about output power of desired harmonics (> -10 dBm), carrier output power (< -50 dBm), RF port return loss (> 10 dB) and isolation from RF port to LO port (> 30 dB). As optimization variables the elements of diode's matching circuit were selected. In Figure 8 are plotted results concerning mixer performance, while in Table 2 are presented numerical results for the related quantities.

Output Power Level (dBm)				Isolation (dB)			Conversion Loss (dB)	RF input Return Loss (dB)
P_{TotIF}	P_{IF} at 5.75 GHz	P_{IF} at 5.85 GHz	P_{IF} at 5.8 GHz	RF to LO	LO to RF	LO to IF		
-8.0	-17.4	-17.2	-64.3	-30.7	-59.3	-68.0	11.4 (8.4)	11.8

Table 2a. Characteristics of the optimized mixer (P_{LO}=+4 dBm, P_{RF}=-5dBm)

LO Frequency (GHz)	$P_{IFTotal}$ (dBm)	P_{IF} (dBm) at $f_{LO}+f_{RF}$	P_{IF} (dBm) at f_{LO}	Conversion Loss (dB)	Return Loss (dB)
5.6	-8.34	-17.6	-32.7	11.7 (8.7)	18.3
5.8	-8.02	-17.2	-64.3	11.4 (8.4)	11.8
6.0	-7.98	-17.6	-41.7	11.9 (8.9)	8.7

Table 2b. Results for three different values of LO frequency in the band 5.2 - 6.4 GHz

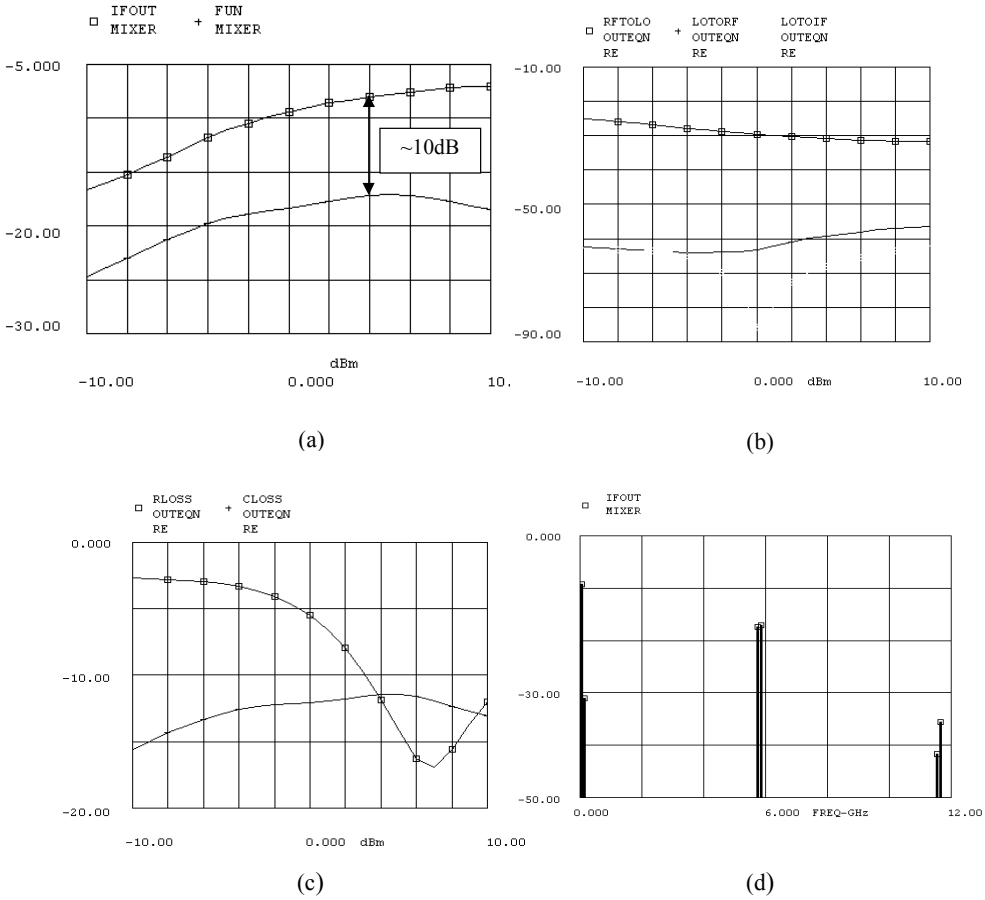


Figure 8. Mixer performance (a) IF output power vs LO power. Total IF power and IF Power at f_{FUN}=5.85 GHz (b) Isolation between ports vs LO power (c) RF input return loss and conversion loss vs LO power (d) Power spectrum of IF output in the dc – 12 GHz band (+4 dBm LO power)

The mixer was also checked in Libra by applying polar pulses in the RF input. In the graphs of Figure 9, the characteristics of input polar pulses are shown along with IF output spectrum from mixer operation. It is noticed that, mixer output contains undesired components from both RF input pulses and harmonics of desired BPSK signal. Thus, the main effort in the next design stage concerned suppression of undesired spectral components in the modulator output.

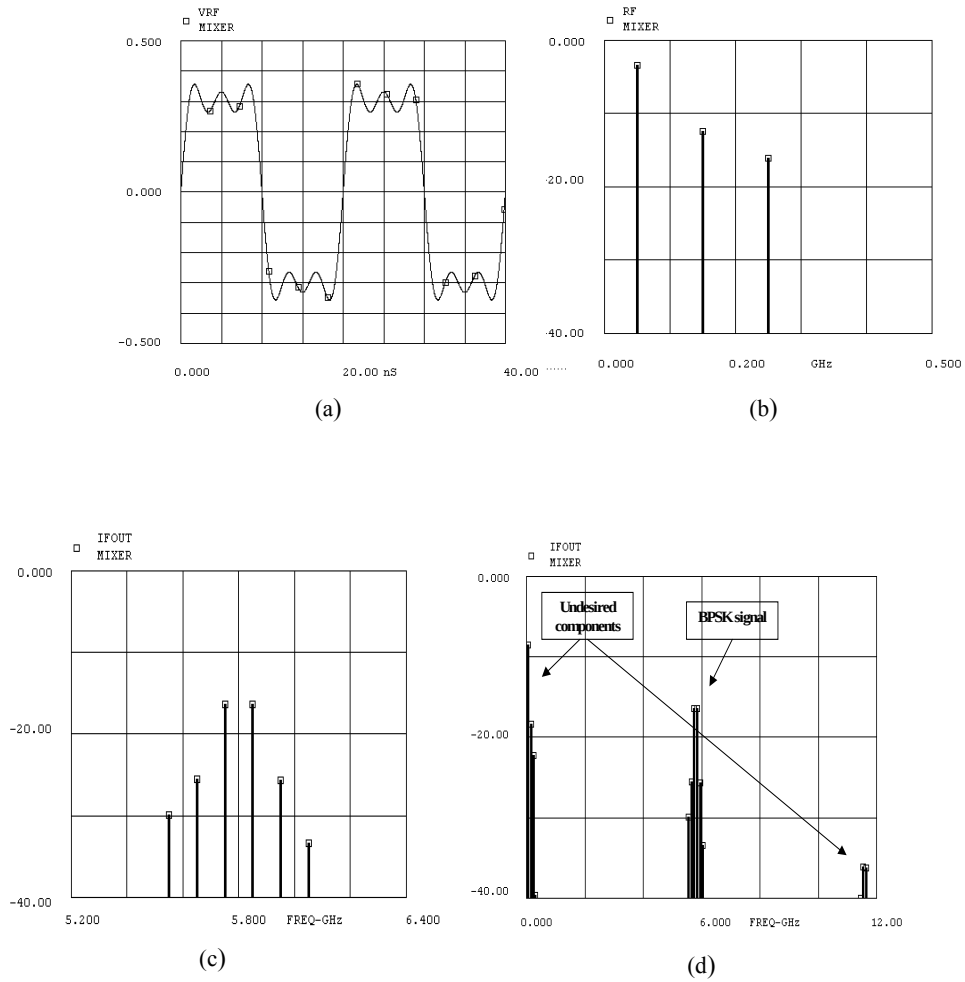


Figure 9. Testing mixer with polar pulses (a) Waveform and (b) Spectrum of of RF input polar pulses (c) Power spectrum of IF output in the 5.2 – 6.4 GHz band (+4 dBm LO power) (d) Power spectrum of IF output in the dc – 12 GHz band (+4 dBm LO power)

5. PERFORMANCE OF QPSK MODULATOR

The circuit of QPSK modulator (Figure 2), contains two rat-race mixes generating the two quadrature BPSK signals. These two signals are multiplexed in the Wilkinson combiner producing the desired Quadrature Multiplexed (QM) QPSK output. Hence, the assembled QPSK modulator was tested with +7dBm LO power level and the final layout of optimized modulator is shown in Figure 10. It is noticed, the presence of $\lambda/4$ short-circuited stubs at the output of the combiner which resulted, as obtained from Figure 11, in acceptable values for both conversion loss and power level of desired QPSK spectral components.

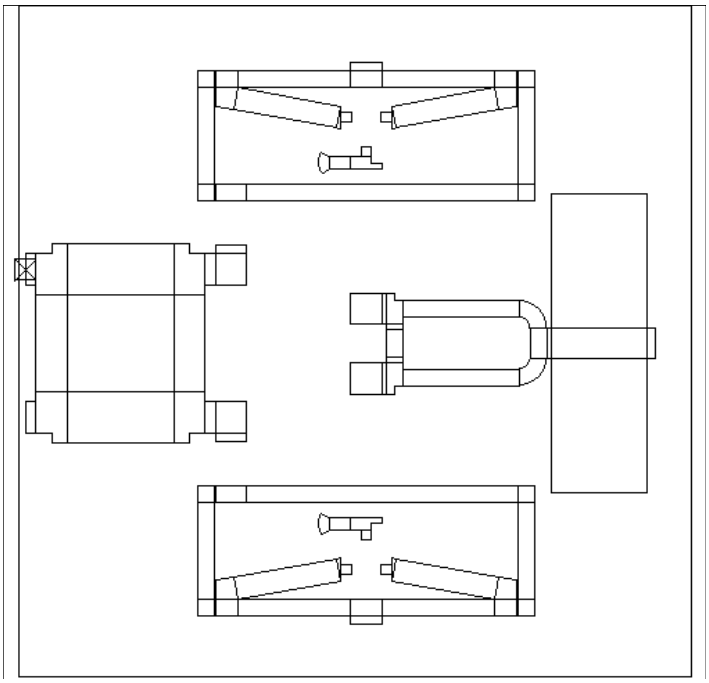
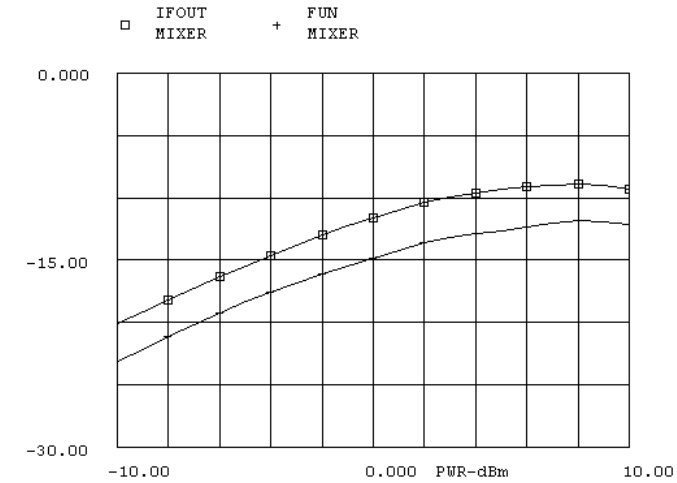


Figure 10. Layout of QPSK modulator (Total area 37.48 mm × 33.5 mm ≈ 1257.6 mm^2).

The modulator was also tested with polar data pulses with results shown in Figure 12, while in Figure 13 plots of return loss and transmission characteristics between ports are presented that have been obtained through linear analysis.



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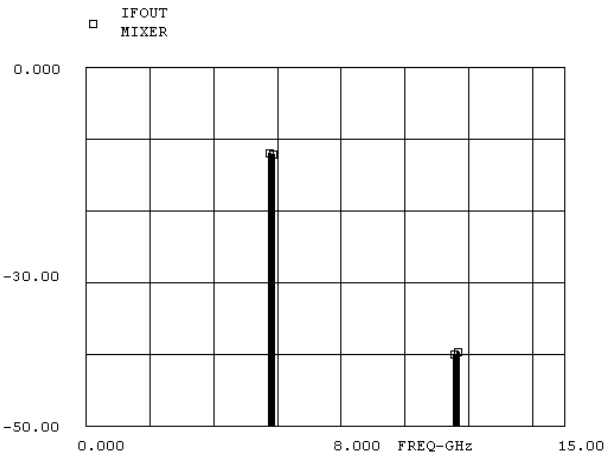

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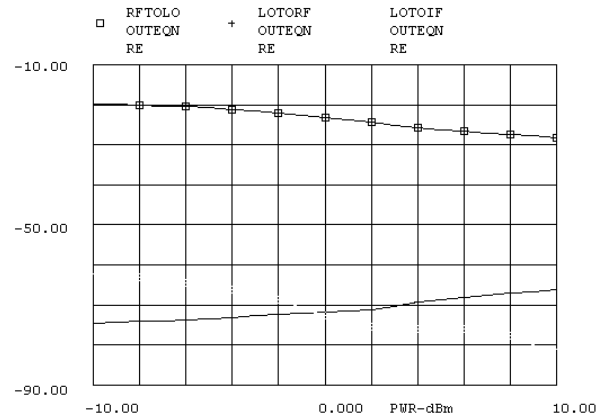
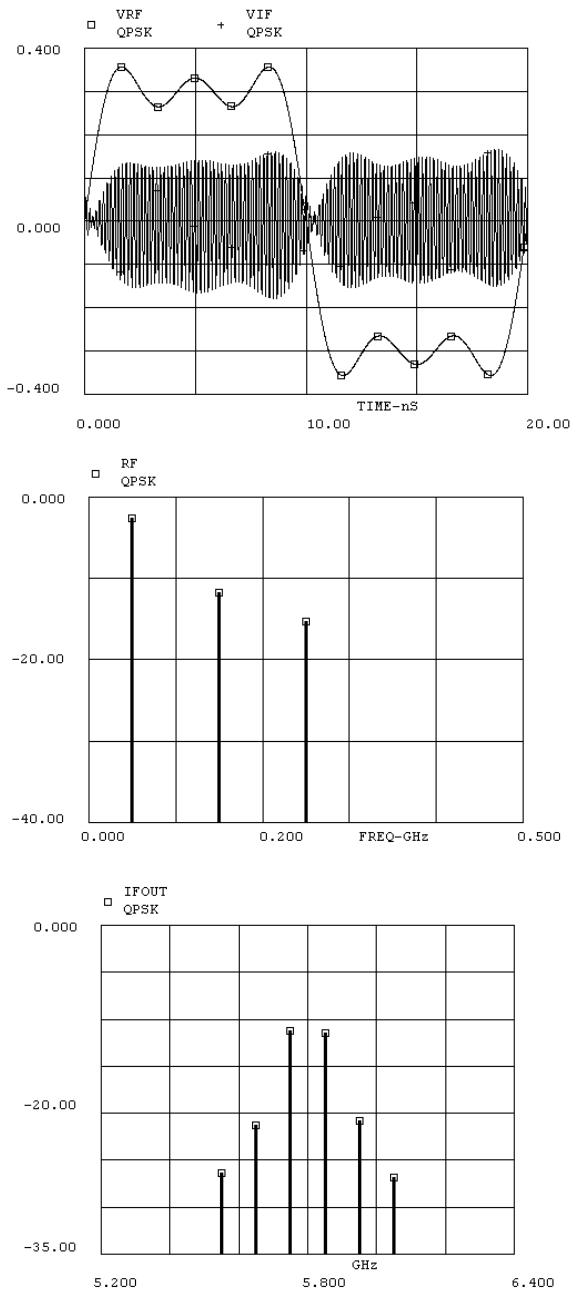


(c)

Figure 11. Performance results from Non-Linear Analysis of optimized QPSK modulator (a) Output power vs LO power, (b) Output Power Spectrum for P_{LO}= +7 dBm, (c) Isolation between ports vs LO power

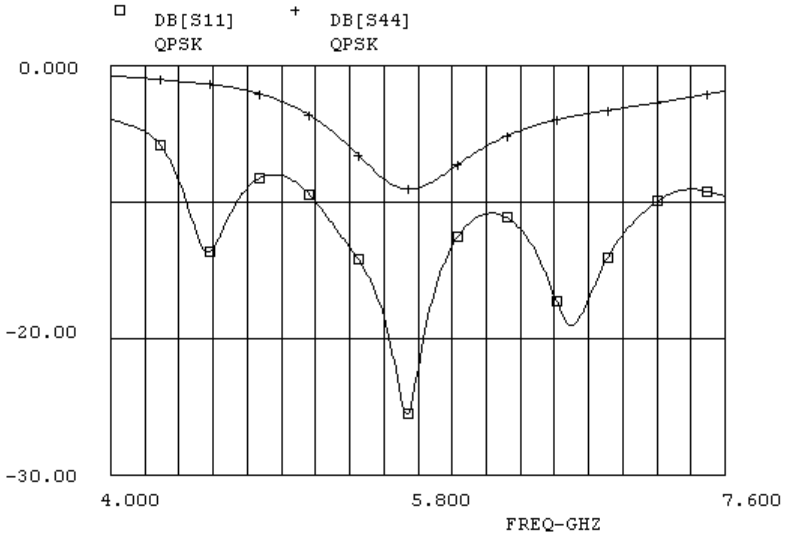


(a)

(b)

(c)

Figure 12. Testing modulator with polar pulses (a) Input and Output Waveforms (Number of harmonics=6), (b) Spectrum of input pulses (Number of harmonics=6), (c) Output Power Spectrum in the 5.2 – 6.4 GHz band (+7 dBm LO power).



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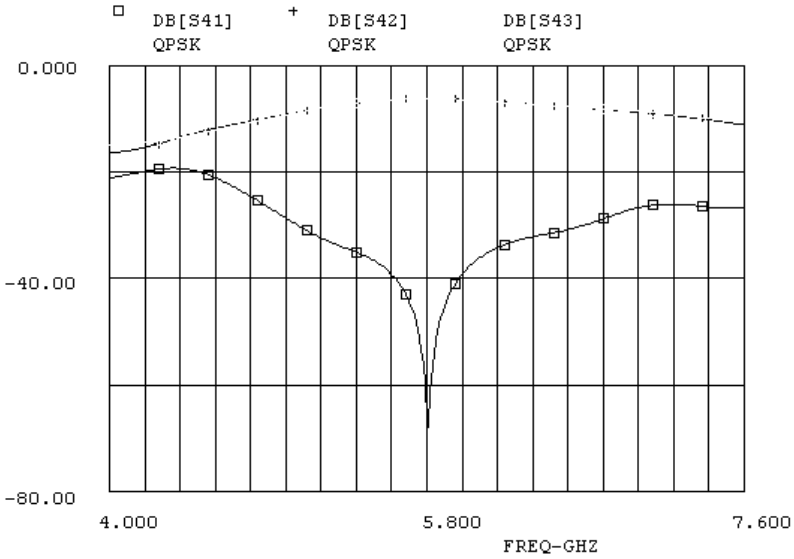

(b)

Figure 13. Performance results (Linear Analysis) (a) Return Loss of LO Input (1) and modulator output (4) (b) Transmission coefficients from inputs to output (s_{41}, s_{42}, and s_{43})

The performance characteristics of the 5.8GHz QPSK modulator are summarized in Table 3. The isolation achieved for both LO-to-RF and LO-to-IF paths is more than 50 dB. The conversion loss obtained is about 16dB, while the carrier compression is 40dB and the compression of undesired harmonics is 30 dB.

Output Power (dBm)				Isolation (dB)		
P_{TotIF}	P_{IF} at 5.75 GHz	P_{IF} at 5.85 GHz	P_{IF} at 5.8 GHz	RF-to-LO	LO-to-RF	LO-to-IF
-8.97	**-11.9**	**-12.0**	**-69.4**	**27.1**	**67.6**	**76.4**

Table 3. Summary of Performance Characteristics (P_{LO}=+7 dBm)

ACKNOWLEDGMENTS

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